Reliability of Ferroelectric Memory for High-Rel and Space Applications

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Introduction

Ferroelectric semiconductor memory technologies have been qualified for commercial production. With high radiation resistance, virtually unlimited endurance,[1] excellent retention over a wide temperature range, and fast programming times, ferroelectric memories provide significant advantages compared to other types of semiconductor nonvolatile memories.

Ferroelectric Memory Design for Reliability

The most common ferroelectric semiconductor memory cells use a ferroelectric capacitor in series with an access transistor, similar to that used in a DRAM.[2] For ferroelectric memories designed for hi-rel environments, two of these cells are used per bit, one programmed to the true logic state and the other programmed to the complement logic state, as shown in Fig. 1. Differential sensing of pairs of cells provides larger margin for hi-rel applications than sensing the switching current of a single cell and comparing it to that of a reference cell.

The ferroelectric material used for the dielectric in these capacitors has the property that internal electric dipoles can exist in two states.[2] Depending on the polarization state of these dipoles, either a logic “one” or logic “zero” is stored. During the first part of the read operation, an interrogation voltage is applied across the ferroelectric capacitor. If the polarization state of the capacitor changes, the resulting switching current charges the bit line. This current is much larger than the linear capacitance current that flows if the ferroelectric capacitor does not switch.

The first part of the read cycle just described is destructive during the read out. During the second part of the read cycle, the true state of the bit must be rewritten to restore the data. It is imperative that the restore portion of every read cycle is completed, even if the power is removed prematurely. Since the read cycle is very fast, typically under 100 ns, adequate charge is stored on the internal nodes to complete the restore portion of the read cycle. Because every read is completed with a rewrite, endurance is based on the number of reads plus the number of writes. Ferroelectric materials that show very little or no fatigue with repeated read/write cycling, such as strontium bismuth tantalate (SBT),[1] are ideal for use in memories designed for high-rel, high-endurance applications.

As with any memory device, ferroelectric memories for high-rel applications should be screened for defective memory cells. Ferroelectric memory cells that cannot be fully polarized and those that do not retain their polarization state for the specified retention period may occur. Special circuitry is used to allow weak writes and reads to be performed on every memory cell in the memory array. By detecting failing bits for weak writes and reads, chips with defective memory cells can be successfully screened using non-destructive electrical testing.

Ferroelectric Technology Reliability

Ferroelectric memory manufacturers use standard process qualification testing. This includes 1000 hour standard operating life and temperature testing. Thermal shock over extended temperature ranges to several hundred cycles, and high humidity pressure cooker tests to over 100 hours, are also used. Endurance is measured by cycling the memory at extended temperatures. A simple technique for assessing endurance is to measure the lowest power supply voltage at which the device will operate after the cycling is completed.[3] If this voltage is compared to the lowest operating voltage prior to read/write cycling, it can be determined if any fatigue has occurred.

During one ferroelectric memory process qualification, using a statistically significant sample size, no failures were observed for high temperature storage, thermal shock and pressure cooker tests. At the same time, only one failure was observed. This failure, observed during life testing, occurred at one of the longest operating times. As compared to EEPROM technology of similar memory density, the reliability of the ferroelectric technology was observed to be comparable or better.

As is typical with other integrated circuit memory, testing at high temperatures can accelerate retention failures in ferroelectric memory. Normal operating temperature failure rates can then be projected by extrapolation. A properly designed retention test will also screen for data imprint. Imprint is the phenomena where a memory cell prefers to remain in a particular polarization state as the result of repeatedly being programmed to that same polarization state. Imprint can be determined by repeatedly programming memory cells to the same polarization state, followed by programming them once to the opposite state, and then testing their ability to remain in that opposite state. Imprint phenomena are observed to be minor in SBT ferroelectrics.

The above technique was used to project failure rates at 27 °C and 70 °C for a 10 year life, as shown in Fig. 2.[4] For memories of both 256-bit and 1K-bit densities, the retention failure rate at 27 °C was projected to be less than 1 FIT and the failure rate at 70 °C was projected to be less than 100 FITs.

Production yield can also be a measure of reliability. Poor yielding processes have sometimes been correlated with poor reliability. Wafer yields of 99.3% have been observed, over 30 production lots, for a device containing a 1K-bit ferroelectric memory.[4]

Radiation Hardness of Ferroelectric Technology

The radiation hardness of ferroelectric memory has been measured for total ionizing doses, neutron exposure, heavy ion exposure and proton irradiation. These results indicate that ferroelectric memory can be used in severe radiation environments. Because the ferroelectric memory storage element is inherently radiation resistant, the hardness of ferroelectric semiconductor memories is primarily limited to the hardness of the underlying CMOS technology.[5]

Total Dose

Ferroelectric thin films which are used for the dielectrics of the storage capacitors in ferroelectric memories have been shown to be tolerant to total ionizing radiation doses up to 100 Mrad (Si) without loss of data.[6-11] This amount of radiation is higher than most CMOS circuitry can tolerate. Therefore, ferroelectric memories intended for high total dose environments must use radiation hardened CMOS circuitry.

Ferroelectric memories use capacitors that are formed after the underlying CMOS transistors are fabricated and before interconnect metalization. These capacitor layers require oxygen anneals at temperatures greater than to 600 °C to form in the proper ferroelectric phase. It has been demonstrated that these anneals have an insignificant effect on the total dose hardness of the CMOS circuitry.[12] Passivation layers are required for stable ferroelectric capacitors. It has also been demonstrated that silicon nitride passivation steps do not significantly degrade the radiation hardness of the CMOS circuitry.[12] Therefore, ferroelectric memories using CMOS circuitry can be designed and processed to withstand total doses in excess of 1 Mrad (Si).

Neutron Exposure

Ferroelectric thin films have been shown to be tolerant to neutron doses up to 10^{15} neutrons/cm^2.[13]

Heavy Ion Exposure

Unbiased ferroelectric 1K-bit embedded memories have been subjected to SEU heavy ion exposure of an effective LET up to 128 MeV-cm^2/mg with no bit failures.[14] Care must be taken in the CMOS design to assure that latch-up does not occur as a result of SEU events. Due to their survival at these levels of heavy ion exposure, ferroelectric memory would be a good choice for use in deep space missions, where severe heavy ion exposure is expected.

Proton Irradiation

Ferroelectric 1K-bit embedded memories have been exposed to proton irradiation in excess of 10^{12} protons/cm^2 with no bit failures.[15]

Conclusions

Ferroelectric memories based on SBT technology have been shown to have reliability levels comparable to other semiconductor memories. Good circuit design allows for memory architectures with considerable margin and testability. Radiation experiments for total ionizing dose, neutrons, heavy ion and proton exposure show the ferroelectric storage element to be radiation tolerant. The radiation hardness of ferroelectric memory is primarily limited by the hardness of the underlying CMOS circuitry.

References

[1] C. A. Paz de Araujo, J. D. Cuchiaro, L. D. McMillan, M. C. Scott and J. F. Scott, “Fatigue-Free Ferroelectric Capacitors with Platinum Electrodes,” *Nature* ***374***, 627 (1995).

[2] R. E. Jones, “Integration of Ferroelectric Nonvolatile Memories,” *Solid State Technology* ***40***, 201 (1997).

[3] T. Sumi, N. Moriwaki, G. Nakane, T. Nakakuma, Y. Judai, Y. Uemoto, Y. Nagano, S. Hayashi, M. Azuma, T. Otsuki, G. Kano, J. Cuchiaro, M. Scott, L. McMillan and C. Araujo, “A 256 kb Nonvolatile Ferroelectric Memory at 3V and 100 ns,” *ISSCC Digest of Technical Papers*, 268 (1994).

[4] Y. Shimada, K. Arita, E. Fujii, T. Nasu, Y. Nagano, A. Noma, Y. Izutsu, K. Nakao, K. Tanaka, T. Yamada, Y. Uemoto, K. Asari, G. Nakane, A. Inoue, T. Sumi, T. Nakakuma, S. Chaya, H. Hirano, Y. Judai, Y. Sasai and T. Otsuki, “Advanced LSI Embedded with FeRAM for Contactless IC Cards and Its Manufacturing Technology,” *Integrated Ferroelectrics* (1999).

[5] J. M. Benedetto, W. M. DeLancey, T. R. Oldham, J. M. McGarrity, C. W. Tipton, M. Brassington and D. E. Fisch, *Radiation Evaluation of Commercial Ferroelectric Nonvolatile Memories, IEEE Trans. Nucl. Sci.* ***NS-38***, 1410-1414 (1991).

[6] G. C. Messenger and F. N. Coppage, “Ferroelectric Memories: A Possible Answer to the Hardened Nonvolatile Question,” *IEEE Trans. Nucl. Sci.* ***NS-35***, 1461-1466 (1988).

[7] J. F. Scott, C. A. Araujo, H. B. Meadows, L. D. McMillan and A. Shawabkeh, “Radiation Effects of Ferroelectric Thin-Film Memories: Retention Failure Mechanisms,” *J. Appl. Phys.* ***66***, 1444-1453 (1989).

[8] J. M. Benedetto, R. A. Moore, F. B. McLean, P. S. Brody and S. K. Dey, “The Effect of Ionizing Radiation on Sol-Gel Ferroelectric PZT Capacitors,” *IEEE Trans. Nucl. Sci.* ***NS-37***, 1713-1717 (1990).

[9] J. R. Schwank, R. D. Nasby, S. L. Miller, M. S. Rodgers and P. V. Dressendorfer, “Total-Dose Radiation-Induced Degradation of Thin Film Ferroelectric Capacitors,” *IEEE Trans. Nucl. Sci.* ***NS-37***, 1703-1712 (1990).

[10] S. C. Lee, G. Teowee, R. D. Schrimpf, D. P. Birnie, D. R. Uhlmann and K. F. Galloway, “Total-Dose Radiation Effects on Sol-Gel Derived PZT Thin-Films,” *IEEE Trans. Nucl. Sci.* ***NS-39***, 2036-2043 (1992).

[11] R. A. Moore, J. M. Benedetto and B. J. Rod, “Total Dose Effect on Ferroelectric PZT Capacitors used as Non-Volatile Storage Elements,” *IEEE Trans. Nucl. Sci.* ***NS-40***, 1591-1596 (1993).

[12] This work was a collaborative effort in 1999 between Celis Semiconductor Corporation and Sandia National Laboratories.

[13] R. A. Moore, J. M. Benedetto, J. M. McGarrity and F. B. McLean, *Neutron Irradiation Effects on PZT Thin Films for Nonvolatile-Memory Applications*, *IEEE Trans. Nucl. Sci.* ***NS-38***, 1078-1082 (1991).

[14] J. M. Benedetto, G. F. Derbenwick and J. D. Cuchiaro, “Single Event Upset Immunity of Strontium Bismuth Tantalate Ferroelectric Memories,” *IEEE Transactions on Nuclear Science* (1999).

[15] The authors would like to thank Gary Swift of Jet Propulsion Laboratory for his collaboration regarding these experiments.

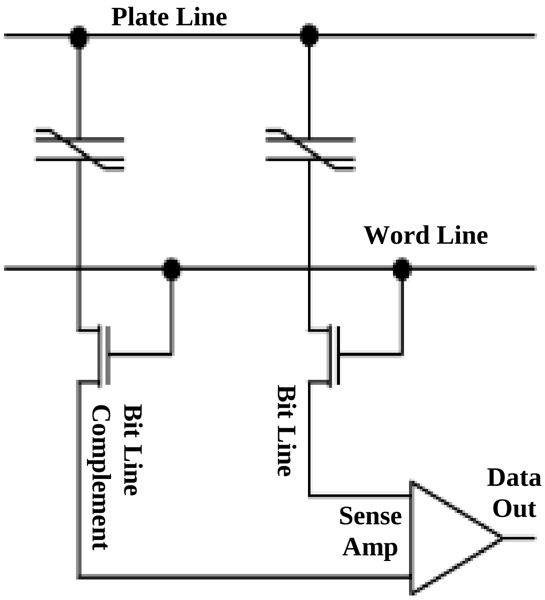

Fig. 1. Differentially Sensed Ferroelectric Memory Cell Schematic

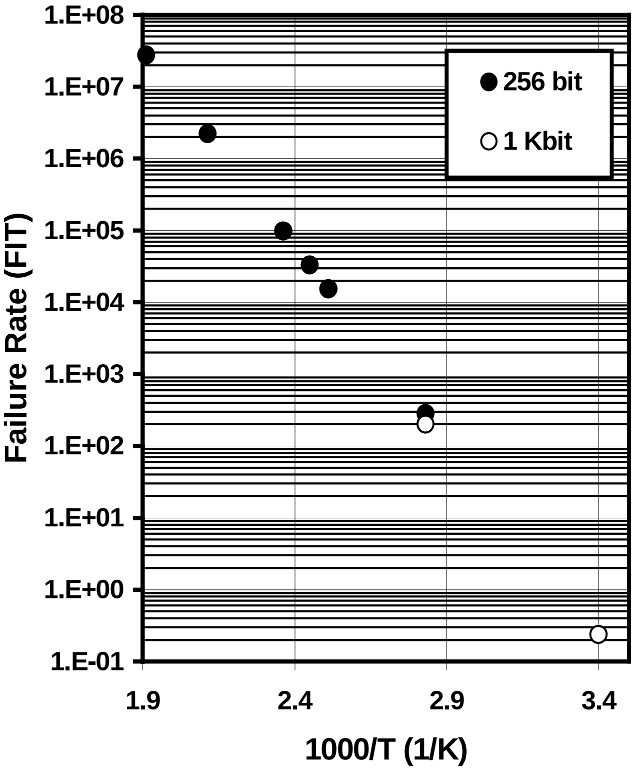

Fig. 2. Retention Failure Rate vs. Reciprocal Temperature for LSIs Containing 256-bit and 1K-bit Ferroelectric Memory[4]