

High Density Radiation Hardened FeRAMs on a 130 nm CMOS/FRAM Process

David A. Kamp, Alan D. DeVilbiss, Gerald R. Haag, Kirk E. Russell and Gary F. Derbenwick
Celis Semiconductor Corporation
Colorado Springs, Colorado
celis@celis-semi.com

Abstract—Using hardened-by-design techniques previously demonstrated on a 1-kbit prototype 0.35-micron ferroelectric semiconductor memory, an 8-kbit FeRAM memory segment has been designed for fabrication on a Texas Instruments 130nm commercial CMOS/FRAM process. The 8-kbit segment can be arrayed to provide radiation hardened ferroelectric memory densities up to 64 Mbit with reasonable chip sizes and radiation hardness vastly superior to that of Flash memory. The 130nm CMOS/FRAM process is capable of wide signal margin, high endurance and long data retention, consistent with the demands of the space market. It is projected from radiation testing of the 1-kbit prototype FeRAM that TID radiation tolerance to greater than 1Mrad(Si) and SEL tolerance to greater than 75 LET can be obtained without the expense and complexity of SOI, and without the need for radiation shielding. A test chip for radiation evaluation has been designed that includes the 8-kbit memory segment, critical boost circuitry, I/O buffers and a number of discrete transistors and devices. The 100 by 300 micron 8-kbit memory segment incorporates a patented, rugged, shunted ferroelectric memory cell that uses a true and complement bit line architecture. The segment read access time is simulated to be 20ns, and read and write cycle times are simulated to be 45ns.

Index Terms—Ferroelectric memory, hardened-by-design, radiation hardened, space applications, adaptability.

I. INTRODUCTION

COMMERCIAL Flash memory with radiation shielding has been used for nonvolatile memory in spacecraft. To date, radiation hardened nonvolatile semiconductor memories have not approached the densities of Flash memory. Previous results on a prototype 1-kbit ferroelectric memory [1] demonstrate that a ferroelectric memory core using ferroelectric storage capacitors combined with hardened-by-design (HBD) CMOS circuitry at 0.35-micron design rules [2], can attain high levels of tolerance to total ionizing dose and single event effects. Preliminary tests indicate that the hardness of the prototype memory exceeds 2 Mrads(Si) total ionizing dose and 163 LET latch-up without the need for shielding.

The recent design of an 8-kbit memory segment in 130 nm

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design rules, which can be used as a building block for memory arrays up to 64 Mbit, demonstrates that hardened-by-design FeRAMs fabricated with scaled CMOS/FRAM technology can approach the densities of Flash memory. The hardened-by-design structures used by Celis have been shown to be compatible with the optical proximity correction (OPC) required for these highly scaled technologies. These radiation hardened FeRAMs can provide fast read access times, write times orders of magnitude faster than Flash memory, almost unlimited endurance, and levels of radiation hardness orders of magnitude higher than for Flash memory.

For the radiation hardened ferroelectric memory core, Celis used its patented shunted ferroelectric memory cell [2] in a true/complement bit line architecture designed to reduce the susceptibility to disturb in harsh environments, such as space applications.

A test chip containing the 8-kbit memory segment, critical circuitry, such as word line boost circuitry, ESD input/output devices and a variety of discrete devices, including transistors, resistors and capacitors, has been designed for fabrication and radiation testing. Simulations of the 8-kbit memory segment provide a segment read access time of 20ns, and segment read and write cycle times of 45ns.

II. FERAM MEMORY SEGMENT

For the ferroelectric memory segment, Celis uses its patented shunted ferroelectric memory cell design with exclusively p-channel transistors [2]. A layout of the memory segment is shown in Figure 1. For maximum immunity to radiation effects, the memory cell incorporates true and complement components containing two transistors and one ferroelectric capacitor in a true/complement bit line memory array architecture. Celis is able to add the shunt transistors to the

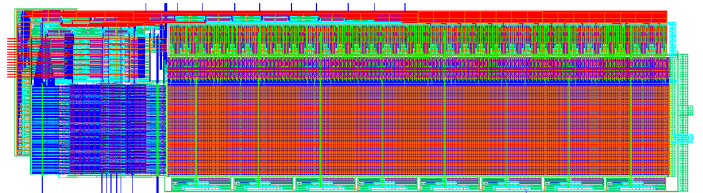


Figure 1. P-Channel Shunted Cell Memory Segment

memory cell components so that the area and aspect ratios of the ferroelectric capacitor and memory cell component are identical to those used in the commercial 130nm CMOS/FRAM process. This assures that the critical wafer fabrication steps for the ferroelectric capacitor are identical to those for the commercial process, and that the reliability of the commercial memory cell related to the process steps is assured for the radiation hardened memory array.

The memory segment also includes sense amplifiers, segment decoders, word line drivers, shunt line drivers and plate line drivers.

III. TEST CHIP

A test chip has been designed for evaluation of the highly scaled radiation hardened FeRAM technology. The test chip containing a few versions of the memory segment also includes other critical circuitry such as word line boost circuitry and input/output buffers. The test chip also contains a variety of discrete devices, such as n- and p-channel transistors of various sizes, resistors, linear capacitors and ferroelectric capacitors.

The purpose of the test chip is to evaluate the Celis HBD techniques and the Texas Instrument 130nm CMOS/FRAM technology for total ionizing dose (TID) radiation hardness prior to producing a 32- or 64-Mbit radiation hardened memory. While some SEU circumvention has been designed into the memory segment, SEU evaluation is not a priority for this effort.

IV. SIMULATIONS OF THE MEMORY SEGMENT

Figure 2 shows a plot of selected waveforms from a simulation of the 8-kbit FeRAM memory segment. A read access time of 20ns and a read cycle time of 45ns are demonstrated at 25°C for nominal simulation models. Figure 3 is a similar plot for a write cycle. The write cycle time is the same as the read cycle time.

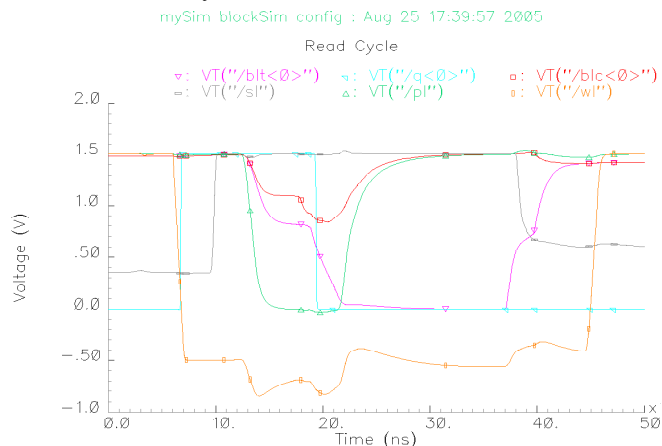


Figure 2. Read Cycle Simulation

The read cycle consists of boosting a selected word line **wl** negative with respect to ground, which turns on the p-channel

access transistor in each memory cell in the selected row. Prior to sensing, the shunt transistors in each of the memory cells in the selected row are turned off via shunt line **sl** being driven to V_{DD} , and the transistors precharging the bit lines (**blt** and **blc**) to V_{DD} are turned off. The plate line **pl** transitions from V_{DD} to 0V producing a bias across the ferroelectric capacitor. One of the two ferroelectric capacitors in each cell switches depending on the logical state of the memory cell, causing the voltage of its corresponding bit line to drop as a result of sharing of the switched and linear charge of the ferroelectric capacitor. The other capacitor of each cell does not switch, causing the voltage of its corresponding bit line to drop to a lesser amount. The drop in bit line voltage for the unswitched capacitor is less than for the switched capacitor because only the linear charge is shared with the bit line. The resulting nominal differential signal between the two bit lines is 275mV. Differentially sensing the memory cell logical state using the true and complement bit lines provides more signal margin than if a differential sense scheme were not used.

The sense amplifier is then enabled by powering it on, pulling the bit line with the lower voltage to ground and the bit line with the higher voltage to V_{DD} . Sensed data is routed to output **q**. The plate line is then returned to V_{DD} , which applies a bias across the switched ferroelectric capacitor to restore it to its original data state. Therefore, every time a memory cell is read, the memory state is refreshed with respect to data

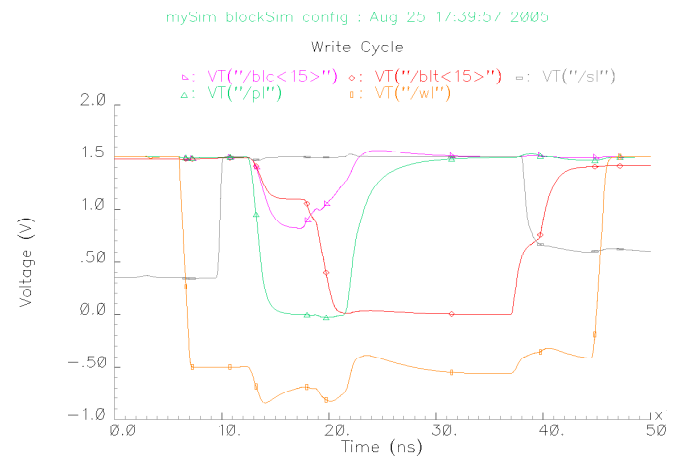


Figure 3. Write Cycle Simulation

retention.

The write cycle is the same as the read cycle except that the bit line signal on selected columns is overwritten prior to the sense amplifier being enabled. Therefore, the read and write cycle times are identical in contrast to those of Flash memory where the write cycles times are orders of magnitude longer than the read cycle times.

The effect of SEU events on the FeRAM must be considered. First, can an SEU event change the polarization state of the ferroelectric capacitor? Previously, it was

measured on a 1-kbit FeRAM memory that no change in polarization of the ferroelectric capacitors was observed to a LET of 128, the maximum LET to which the FeRAM was tested [3], [4]. In contrast, a DRAM is vulnerable to single event upset because the stored charge can be overwritten by charge from a particle strike.

Secondly, can an SEU event affect the written or read state of a bit because of the destructive read out (DRO) cycle used to read an FeRAM bit? A vulnerability to an SEU strike exists during sensing when the polarization switched charge is shared to the bit line capacitance. For FeRAM, the time window of vulnerability to single event upset begins with the plate line transition low and ends with the enabling of the sense amplifier. Figure 2 shows the time for which this vulnerability exists is 5ns. If a strike of a source/drain region connected to a bit line occurs within this time period, and if the strike produces an amount of charge exceeding the differential charge produced by the memory cell, then incorrect sensing can occur, and the incorrect logical state is programmed into the memory cell when the sense amplifier is enabled.

Error detection and correction circuitry either on-chip or off-chip is utilized to mitigate the DRO SEU vulnerability. Periodic scrubbing of the memory is also desirable. As the design rule of the technology is scaled to smaller dimensions, the amount of polarization switched charged stored on the capacitor is reduced, and the vulnerability increases. Proper partitioning of the memory array can reduce this vulnerability. Design of the memory array using p-channel transistors in an n-well mitigates some of the sensitivity because a portion of the charge deposited by the SEU particle is absorbed at the n-well/substrate junction.

V. HARDENED-BY-DESIGN TECHNIQUES

Celis uses a number of hardened-by-design techniques to manufacture a radiation hardened semiconductor memory on the 130nm commercial Texas Instrument CMOS/FRAM production line that uses no special processing for radiation hardness. The HBD techniques must be compatible with the OPC data processing needed to fabricate the reticles so that the actual geometries of the structures printed on the silicon are similar to those designed. For example, simple ring structure annular n-channel transistors that have been used in prior designs [1] are not compatible with the OPC required at the 130nm technology node.

Some of the techniques used by Celis for the 130nm technology node for TID, SEL and SEU immunity include:

- p-channel transistors in memory array
- special n-channel gate structures
- p-type guard rings
- robust/redundant logic gates protecting latches
- SEE immune latches and sense amplifiers
- no charge pumps

These HBD layout techniques, proven in HBD designs, were added under the guidance of sophisticated rule and structure checking software developed by Celis for the prototype chip design.

VI. CONCLUSION

Use of a 130nm commercial CMOS/FRAM wafer fabrication process with hardened-by-design techniques allows ferroelectric memories up to 64 Mbit in density to be realized. Simulations show nominal read access and cycle times to be 20ns and 45ns, respectively. Radiation hardness levels in excess of 1 Mrad(Si) for TID and 75 LET for SEL are expected.

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David A. Kamp (M'78) received the B.S. degree in electrical engineering from the University of Michigan in 1981.

In 1996, he joined Celis Semiconductor Corporation in Colorado Springs, Colorado, where he is Vice President of Design and Chief Operating Officer responsible for the design, development and production of ferroelectric memory products. These products include RFID and memory for both space and terrestrial applications. Over the last 10 years, his focus has been the design and development of ferroelectric memories. He has designed ferroelectric memories for Ramtron International and Ceram. From 1987 through 1994, he designed nvSRAM and EEPROM memories for Simtek Corporation. From 1981 until 1987, he was employed at Inmos Corporation in Colorado Springs, Colorado, where he worked in the product engineering of EEPROM, SRAM and DRAM. He has 10 issued patents in the area of memory design.



Alan D. DeVilbiss received the B.S. degree in physics from the University of Colorado in 1993.

He joined Celis Semiconductor Corporation in Colorado Springs, Colorado in 1998. He is a Senior Design Engineer involved in the design, development, and testing of ferroelectric memories. He has numerous technical publications and holds patents in the areas of ferroelectric memory design and ferroelectric device testing and characterization. He is also involved in analog and mixed signal CMOS design and has several patent applications pending for integrated circuit designs for contactless radio frequency identification tags and cards. From 1994 to 1998 he was a Staff Scientist at Symetrix Corporation in Colorado Springs, Colorado, where he was in charge of the test and measurement laboratory. From 1991 to 1993, he participated in research in non linear optics at Seiler Research Laboratory at the US Air Force Academy as a college student and Graduate Research Associate. He has several issued and pending patents.



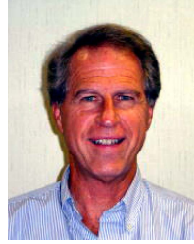
Gerald R. Haag received the B.S. degree in electrical engineering from South Dakota State University in 1972, and the M.S. degree in engineering from South Dakota State University in 1978.

In 2004, he joined Celis Semiconductor Corporation in Colorado Springs where he is a Senior Design Engineer. From 2003 to 2004 at Semquest Incorporated, he designed and tested a security-imaging chip. From 2001 through 2004 he worked as an independent contractor. He joined LSI Logic Corporation in 1993 to design, develop and support SRAM, dual-port RAM, ROM, DRAM, and CAM memory compilers for the NCR and Symbios Logic ASIC libraries. In 1991 he joined SIMTEK to test and to qualify nvSRAM memories. From 1983 to 1991 at Digital Equipment Corporation he provided product development support for uVAX / CVAX product line peripheral chips and designed drive electronics chips. He joined MOSTEK in Carrollton, Texas in 1978 to provide product development and support for telecommunications chips. He is an inventor on two patents.



Kirk E. Russell received the B.S degree in electrical engineering from North Carolina State University in 1996 and the Master's of Science in electrical engineering from North Carolina State University in 1998.

In 2004, he joined Celis Semiconductor in Colorado Springs where he is a Design Engineer. Between 2004 and 2001 he worked as an independent contractor. From 2001 to 2000 at Colorado MicroDisplay he designed, laid out and tested a SVGA microDisplay. He joined Lockheed Martin in 1999 to work on a radiation hardened redesign of a PowerPC core for the Teledesic satellite phone system. In 1998 he was employed at Cadence Design Systems working on Ethernet, SERDES and audio chips. During 1997 he was employed at IBM in the Networking Hardware Division working on a 100Tx Ethernet chip.



Gary F. Derbenwick received the B.S. degree in electrical engineering from the University of Connecticut in 1962, the M.S. degree in electrical engineering from Stanford University in 1967, and the Ph.D. degree in electrical engineering from Stanford University in 1970.

In 1996, he was a founder of Celis Semiconductor and is President and CEO. In 1986 he founded, with Dr. Richard Petritz, Simtek Corporation, a semiconductor company focused on high performance nvSRAMs. In 1980, he became Process Technology Development Manager at Inmos Corporation where he worked on the development of DRAMs, SRAMs, EEPROMs and microprocessors, and pioneered the use of silicon nitride as the dielectric in DRAM storage capacitors and the use of zero drain overlap transistors for high speed circuits. He joined Sandia National Laboratories in 1974 where he developed one of the first radiation hardened CMOS processes and was instrumental in developing the radiation hardened SRAMs used in the Galileo spacecraft. He joined Bell Laboratories in Murray Hill, New Jersey in 1970 where he and Dr. Richard Powell demonstrated that holes were mobile in SiO₂ leading the way to the development of radiation hardened CMOS circuits. He is an author of over 70 technical papers, an author of two book chapters, and an inventor on over 10 patents. Dr. Derbenwick twice received outstanding paper award at the IEEE Nuclear and Space Radiation Effects Conference.